


Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. MI22-2426		SERIAL NO. 10/690,029	
				LIST OF ART CITED BY APPLICANT (Use several sheets if necessary)			
				APPLICANT: Garo J. Derderian et al.			
				FILING DATE October 20, 2003		GROUP 2812	

U.S. PATENT DOCUMENTS							
Examiner's Initials	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
h	AA	6,753,618	06/2004	Basceri et al.	257	915	//
	AB	5,470,794	11/1995	Anjum	437	200	//
	AC	2003/0219942 A1	11/2003	Choi et al.	438	253	//
	AD	2004/0245560 A1	12/2004	Pontoh et al.	257	309	//
	AE	2004/0245559 A1	12/2004	Pontoh et al.	257	306	//
	AF	2004/0046197 A1	03/2004	Basceri et al.	257	296	//
	AG	2004/0043228 A1	03/2004	Derderian et al.	428	446	//
	AH	2003/0213987 A1	11/2003	Basceri et al.	257	296	//
h	AI	2003/0205729 A1	11/2003	Basceri et al.	257	200	//


FOREIGN PATENT DOCUMENTS							
Document Number	Date	Country	Class	Subclass	Translation		
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
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EXAMINER <i>Ruor H. ang</i>	DATE CONSIDERED <i>3/2005</i>
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Form PTO-1449		U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE		ATTY. DOCKET NO. M122-2426		SERIAL NO. 10/690,029	
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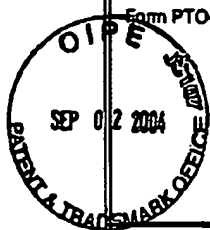
U.S. PATENT DOCUMENTS							
Examiner's Initials	Class	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate
h	AA	3,349,474	12/1963	D. H. Rauscher	—	—	—
	AB	5,904,517	05/1999	Gardner et al.	438	197	—
	AC	5,998,264	12/1999	Wu	438	260	—
	AD	6,180,465 B1	01/2001	Gardner et al.	438	291	—
	AE	6,207,485 B1	03/2001	Gardner et al.	438	216	—
h	AF	6,548,854 B1	04/2003	Kizilyalli et al.	257	310	—
	AG						
h	AH	2003/0045060 A1	03/2003	Ahn et al.	438	287	—
h	AI	2003/0045078 A1	03/2003	Ahn et al.	438	585	—

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Examiner's Initials	Class	Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
h	AJ	EP 0 851 473 A2	01/1998	EPO	—	—	X	
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)			
h	AM		Chang et al., Silicon surface treatments in advanced MOS gate processing, Microelectronic Engineering, (2004), pages 130-135
h	AN		Lemberger et al., Electrical characterization and reliability aspects of zirconium silicate films obtained from novel MOCVD precursors, Microelectronic Engineering (2004), pages 315-320
h	AO		Lu et al., Effects of the TaN, interface layer on doped tantalum oxide high-k films, VACUUM (2004), pages 1-9.

EXAMINER <i>Wen Huang</i>	DATE CONSIDERED <i>9/20/03</i>
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U.S. PATENT DOCUMENTS								
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w	AA	4,086,074	04/78	Minot et al.				
	AB	4,622,735	11/86	Shibata				
	AC	4,683,645	08/87	Naguib et al.				
	AD	4,693,910	09/87	Nakajima et al.				
	AE	4,766,090	08/88	Coquin et al.				
	AF	5,099,304	03/92	Takemura et al.				
	AG	5,236,865	08/93	Sandhu et al.				
	AH	5,444,024	08/95	Anjum et al.				
w	AJ	5,470,784	11/95	Anjum et al.				
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		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
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w	AA	ABSTRACT: Bascari et al., Atomic Layer Deposition for Nanoscale CU Metalization, 10 pages (pre-April 2004).						
w	AB	En et al., Plasma immersion ion implantation reactor design considerations for oxide charging, 85 SURFACE AND COATINGS TECHNOLOGY 64-69 (1986).						
w	AC	Ku et al., The Application of Ion Beam Mixing, Doped Silicide, and Rapid Thermal Processing of Self-Aligned Silicide Technology, 137 J. Electrochem. Soc. No. 2, pp. 728-740 (February 1990).						
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Gara Hwang		3/2005						
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Examiner's Initials	Class	Document Number	Date	Name	Class	Subclass	Filing Date if Appropriate	
m	AA	2001/0006759 A1	07/01	Shipley, Jr. et al.	1	1	---	
l	AB	2002/0076879 A1	06/02	Lee et al.	1	1	---	
w	AC	2002/0196651 A1	12/02	Weis	1	1	---	
w	AD	2003/0013272 A1	01/03	Hong et al.	1	1	---	
	AE							
	AF							
	AG							
	AH							
	AI							
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m	AA	10/609,311	Yates			06/03	
l	AB	10/655,997	Daley			09/03	
l	AC	10/689,958	Basceri			10/03	
v	AD	10/882,118	Sandhu et al.			04/04	
h	AE	10/879,367	Blalock et al.			06/04	
	AF						
	AG						
	AH						
	AI						

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h	AA	5,670,298	09/97	Hur			
	AB	6,037,239	03/00	Jennings			
	AC	6,096,621	08/00	Jennings			
	AD	6,130,140	10/00	Gonzalez			
	AE	6,133,105	10/00	Chen et al.			
	AF	6,133,116	10/00	Kim et al.			
	AG	6,177,235 B1	01/01	Francou et al.			
	AH	6,277,709 B1	08/01	Wang et al.			
h	AI	6,277,728 B1	08/01	Ahn et al.			

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h	AM	ABSTRACT: How to Eliminate Voiding in Porous-Low-k Dielectrics and The Mechanism of Void Formation; Lin et al.; 4 pages
h	AN	COB Stack DRAM Cell Technology beyond 100 nm Technology Node; Yongjik Park & Knam Kim; pp. 349.1 - 349.3;
h	AO	Rubin et al., Shallow-Junction Diode Formation by Implantation of Arsenic and Boron Through Titanium-Silicide Films and ..., 17 IEEE Transactions on Electron Devices, No. 1, pp. 183-190 (January 1990).

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DATE CONSIDERED

3/2005

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h	AA	6,440,793 B1	08/02	Divakaran et al.			—
	AB	6,465,325 B2	10/02	Ridley et al.			—
	AC	6,720,638 B2	04/04	Tran			—
	AD	6,780,728 B2	08/04	Tran			—
	AE	6,156,674	12/00	Li et al.			—
	AF	6,281,100 B1	08/01	Yin et al.			—
	AG	6,291,363 B1	09/01	Yin et al.			—
	AH	6,380,611 B1	04/02	Yin et al.			—
h	AI	6,383,723 B1	05/02	Iyer et al.			—

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G. H. Hwang

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